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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,877	11/21/2003	Shih Wei Wang	TS02-622	1485

7590 05/04/2005

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EXAMINER	
ROSE, KIESHA L	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 05/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,877	WANG ET AL.	
	Examiner	Art Unit	
	Kiesha L. Rose	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the filing of the application.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

Fig. 1, #20

Fig. 3, #40

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to because in Figs. 1 and 2 #22 is suppose to be the edges and #20 is the arrows but the drawings have #22 pointed to the arrows.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the transfer gate stack must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 8 recites the limitation "top gate stack layer" in Claim 8. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-7, 9 and 21-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurooka et al. (U.S. Patent 6,184,088).

Kurooka discloses a split gate transistor (Fig. 10) that contains a semiconductor region within a substrate (2), source (3) and drain (4) regions contained within said semiconductor region, at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer (6) formed over said semiconductor region, a conductive gate layer (70) disposed over said gate insulator layer, with nitrogen atoms (70a) incorporated along the conductive gate layer sidewall

The semiconductor region (region where source and drain are) is a silicon region, the substrate (2) is a silicon substrate, the gate insulator layer (6) is an oxide layer, the conductive gate layer (70) is a polysilicon layer, the conductive gate layer is a gate of a semiconductor integrated circuit device and the nitrogen atoms (70a) extend to the conductive gate layer-gate insulator layer interface in the vicinity of the conductive gate layer edge

Regarding claim 27, a top gate stack (19) is formed over conductive gate layer and an oxide sidewall insulator layer (8) is formed over sidewalls of gate stack

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

> the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurooka in view of Applicant's Prior Art (Figure 1).

Kurooka discloses all the limitations except for a top gate layer disposed on the conductive gate layer and sidewall insulator layer. Whereas Applicant's Prior Art (Fig. 1) contains a semiconductor region within a substrate (2), source and drain regions (4) contained within said semiconductor region, at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer (6) formed over said semiconductor region, a conductive gate layer (8) over said gate insulator layer, a control gate (10) a sidewall insulator layer (16) and a top insulator layer (14) and with disposed over sidewalls of said gate stack. The top insulator is formed to insulate the control gate. (Page 3, lines 1-2) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Kurooka by incorporating a top gate stack to insulate the control gate as taught by Applicant's Prior Art (Fig. 1).

Claims 10-20, 30-37 and 39-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art (Fig. 1) in view of Kurooka.

Applicant's Prior Art contains a split gate transistor (Fig. 1) that contains a semiconductor region within a substrate (2), source and drain regions (4) contained within said semiconductor region, at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer (6) formed over said semiconductor region, a conductive floating

gate layer (8) over said gate insulator layer, an interpoly insulator layer (12) disposed over said conductive gate layer, a conductive control gate layer (10), a sidewall insulator layer (16) and a top insulator layer (14) disposed over sidewalls of said gate stack

The semiconductor region is a silicon region, the substrate (2) is a silicon substrate, the gate insulator layer (6) is an oxide layer, the conductive floating gate layer (8) is a polysilicon layer, the conductive floating gate layer is a gate of a split gate, the interpoly insulator (12) is an ONO layer, sidewall insulator layer (16) is an oxide, the conductive control gate layer (10) is a polysilicon layer and the top gate stack (14) is an oxide

Applicant's Prior Art (Figure 1) discloses all the limitations except for nitrogen atoms incorporated along the conductive floating gate layer sidewall. Whereas Kurooka discloses a split gate transistor (Fig. 10) that contains a semiconductor region within a substrate (2), source (3) and drain (4) regions contained within said semiconductor region, at least a gate stack, disposed over said semiconductor region, situated between said source and drain regions and containing a gate insulator layer (6) formed over said semiconductor region, a conductive floating gate layer (70) disposed over said gate insulator layer, with nitrogen atoms (70a) incorporated along the conductive floating gate layer sidewall and a sidewall insulator (8) and a transfer gate stack (41a)(Fig. 11a) comprising a gate insulator (6), a conductive transfer gate layer (70) that is polysilicon disposed over gate insulator layer that is situated between the gate stack and the source region (3). Where the nitrogen atoms are incorporated along the conductive floating gate layer sidewall-sidewall insulator layer interface and the

conductive floating gate layer-gate insulator layer interface in the vicinity of the conductive floating gate layer edge. The nitrogen atoms are formed on the sidewall of the conductive floating gate layer to minimize the dangling bond of the native oxide film and to prevent bird's beak from being formed on the tunnel insulating layer. (Column 9, lines 4-24) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Applicant's Prior Art by incorporating nitrogen atoms on the sidewall of the floating gate to minimize the dangling bond of the native oxide film and to prevent bird's beak from being formed on the tunnel insulating layer as taught by Kurooka.

Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kurooka in view of Aminzadeh et al. (U.S. Patent 5,827,769).

Kurooka discloses all the limitations except for how the nitrogen treatment is formed. Whereas Aminzadeh discloses a transistor (Figs. 7-8 and 15) that contains a nitride treatment layer (1000) where the treatment is a RTA (rapid thermal processing) or furnace annealing where the RTA process is used with NH3 at a temperature of about 1000 degrees for about 10 seconds. The RTA process is used to increase wafer to wafer uniformity due to the elimination of furnace position variability and to reduce impact on the process thermal budget due to shorter temperature ramp times. (Column 4, lines 32-40) (Column 6, lines 1-15) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Kurooka by incorporating the RTA process for the nitration treatment to increase wafer to wafer uniformity due to the elimination of furnace position variability

and to reduce impact on the process thermal budget due to shorter temperature ramp times as taught by Aminzadeh.

Claim 38 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Prior Art and Kurooka in view of Aminzadeh et al. (U.S. Patent 5,827,769).

Applicant's Prior Art and Kurooka disclose all the limitations except for how the nitrogen treatment is formed. Whereas Aminzadeh discloses a transistor (Figs. 7-8 and 15) that contains a nitride treatment layer (1000) where the treatment is a RTA (rapid thermal processing) or furnace annealing where the RTA process is used with NH3 at a temperature of about 1000 degrees for about 10 seconds. The RTA process is used to increase wafer to wafer uniformity due to the elimination of furnace position variability and to reduce impact on the process thermal budget due to shorter temperature ramp times. (Column 4, lines 32-40) (Column 6, lines 1-15) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Applicant's Prior Art and Kurooka by incorporating the RTA process for the nitration treatment to increase wafer to wafer uniformity due to the elimination of furnace position variability and to reduce impact on the process thermal budget due to shorter temperature ramp times as taught by Aminzadeh.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLR

AMIR ZARABIAN
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